MAY 1985 – REVISED NOVEMBER 1985

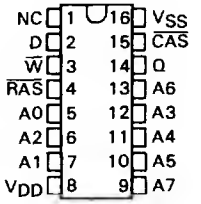
This Data Sheet Is Applicable to All TMS4164s Symbolized with Code "A" as Described on Page 4-57.

- 65,536 X 1 Organization
- Singla 5-V Supply (10% Tolaranca)
- JEDEC Standardizad Pinout in Dual-in-Lina Packaga
- Parformanca Ranges:

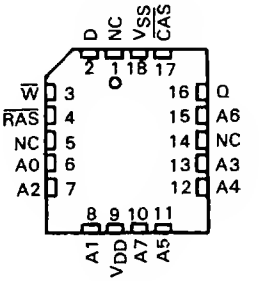
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME CDLUMN ADDRESS (MAX)	READ DR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4164-12	120 ns	70 ns	230 ns	255 ns
'4164-15	150 ns	85 ns	260 ns	290 ns
'4164-20	200 ns	135 ns	330 ns	345 ns

- Upward Pin Compatibla with TMS4116 (16K Dynamic RAM)
- First Military Varsion of 64K DRAM
- Also Availabla with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), S(−55°C to 100°C), or M(−55°C to 125°C) Tamperatura Rangas
- Operations of the TMS4164 Can Ba Controllad by TI's TMS4500A and/or THCT4501 Dynamic RAM Controllers
- Long Rafrash Parlod . . . 4 ms
- Low Rafresh Ovarhaad Tima . . . As Low As 1.8% of Total Rafrash Pariod
- All Inputs, Outputs, Clocks Fully TTL Compatibla
- 3-Stata Unlatchad Output
- Common I/O Capability with Early Writa Faatura
- Paga-Moda Oparation for Fastar Accass
- Low Powar Dissipation
  - Oparating . . . 135 mW (Typ)
  - Standby . . . 17.5 mW (Typ)
- SMOS (Scalad-MOS) N-Channal Tachnology

N PACKAGE
(TOP VIEW)



FP PACKAGE
(TDP VIEW)



PIN NDMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4164 is a high-speed, 65,536-bit, dynamic random-access memory, organized as 65,536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS4164 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation is 135 mW typical operating and 17.5 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility. Pin 1 has no internal connection to allow compatibility with other 64K RAMs that use this pin for an additional function.

The TMS4164 is offered in 16-pin dual-in-line plastic (N suffix) and 18-lead plastic chip carrier (FP suffix) packages. The dual-in-line plastic package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers. The TMS4164 is guaranteed for operation from 0°C to 70°C.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the ouput buffer is in the high-impedance state unless $\overline{CAS}$ is applied, The $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

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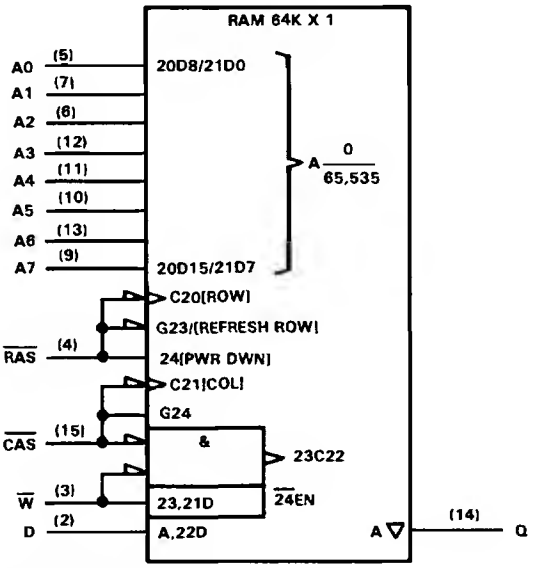
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

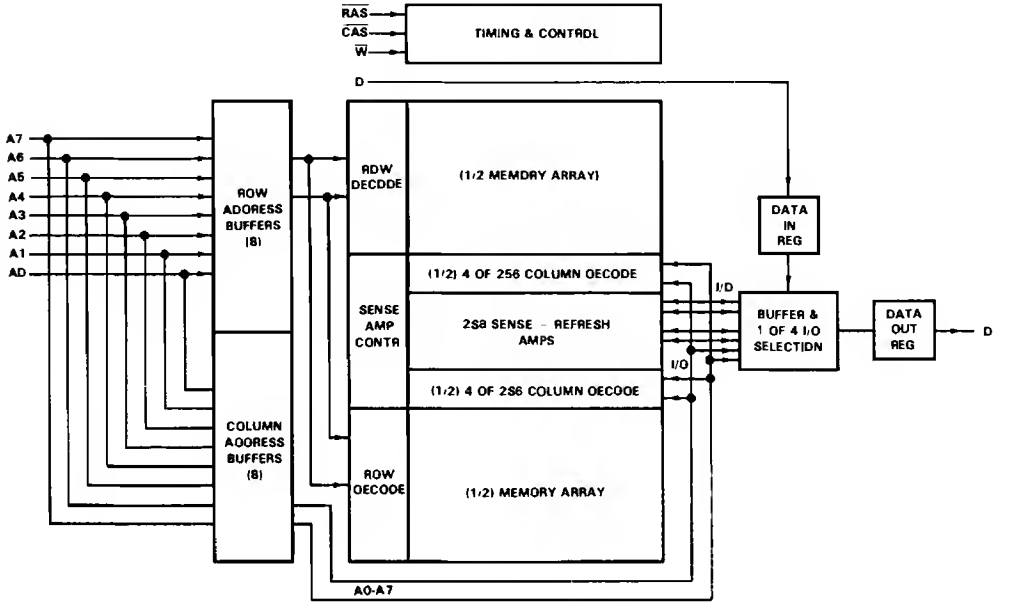
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1)	−1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS}	−1 V to 6 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies"* in Section 12.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}		V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		6	
V_{IL}	Low-level input voltage (see Notes 3 and 4)		−0.6		0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

4. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TMS4164-12			TMS4164-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		40	48		35	45	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		28	40		25	37	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		28	40		25	37	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ Additional information on page 4-58.
§ V_{IL} > −0.6V. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4164-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		27	37	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		20	32	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		20	32	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ Additional information on page 4-58.
§ $V_{IL} > -0.6V$. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	pF
$C_{i(RC)}$	Input capacitance strobe inputs	6	8	pF
$C_{i(W)}$	Input capacitance, write enable input	6	8	pF
C_o	Output capacitance	5	6	pF

† All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4164-12		TMS4164-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{A(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		70		85	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	C_L = 100 pF, t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	40	ns

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4164-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	C_L = 100 pF, t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range (see Note 1)

		ALT. SYMBOL	TMS4164-12		TMS4164-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	130		145		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	255		290		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	70	10,000	85	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	−5		−5		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	85		95		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	40		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	85		95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	40		45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	40		45		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	85		95		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	70		85		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	40		60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	15	50	20	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	110		120		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 1: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (see Note 1)

		ALT. SYMBOL	TMS4164-20 MIN	TMS4164-20 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	−5		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	120		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	145		ns
$t_{h(WLD)}$	Date hold time after $\overline{W}$ low	t_{DHW}	55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	145		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	130		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 1: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

PARAMETER MEASUREMENT INFORMATION

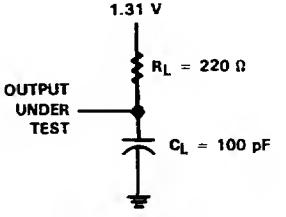
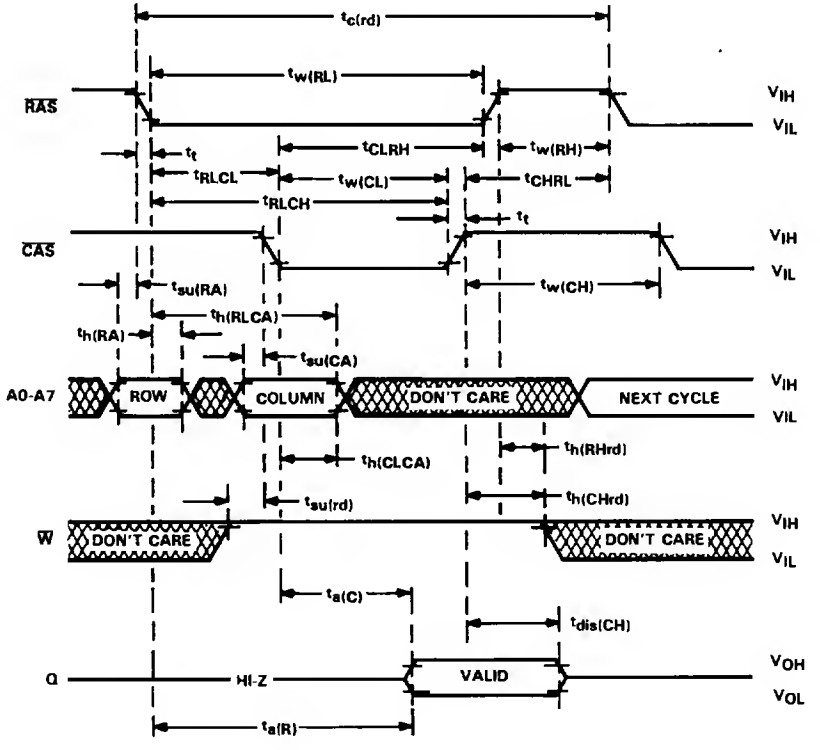


FIGURE 1. LOAD CIRCUIT

read cycle timing



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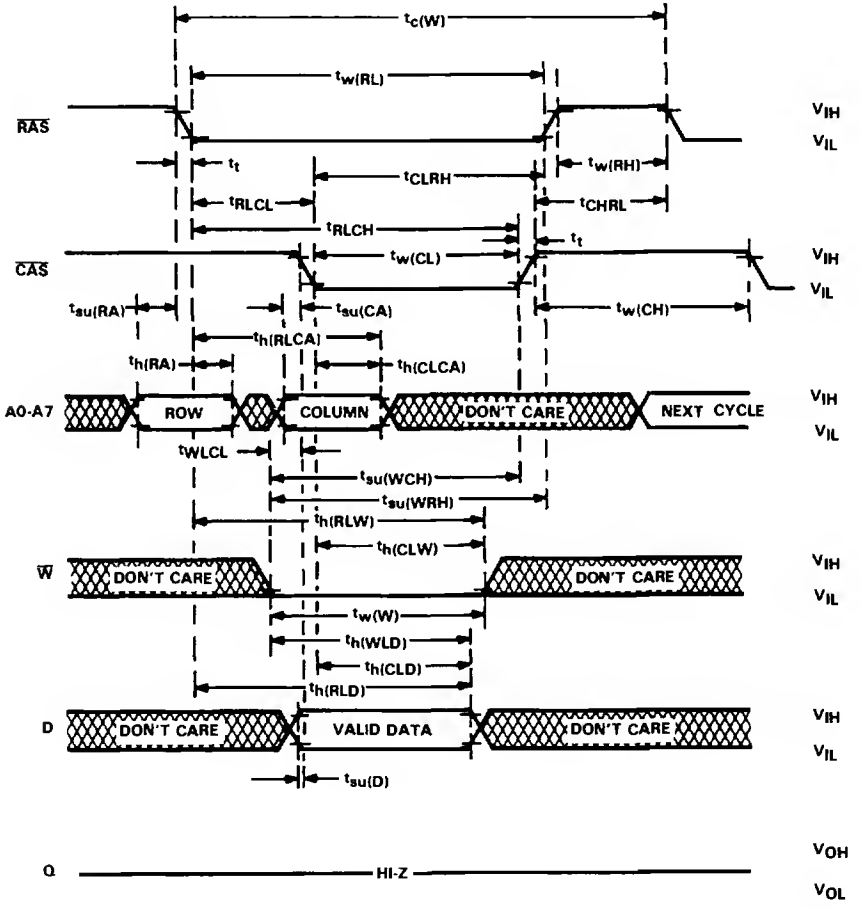
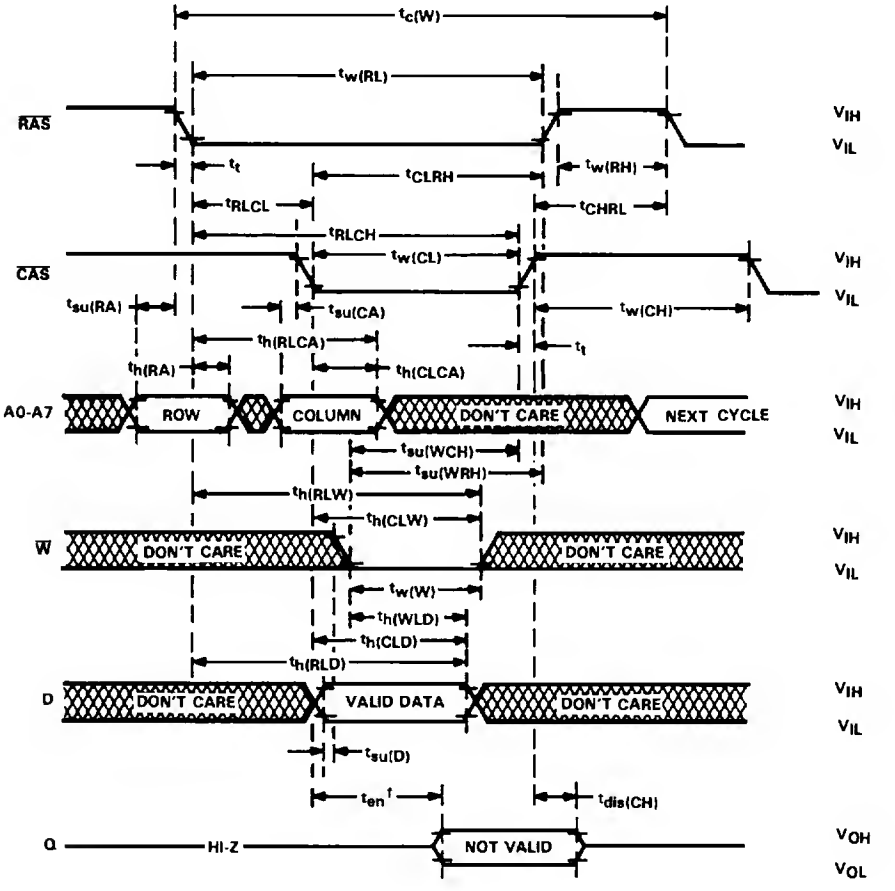
early write cycle timing

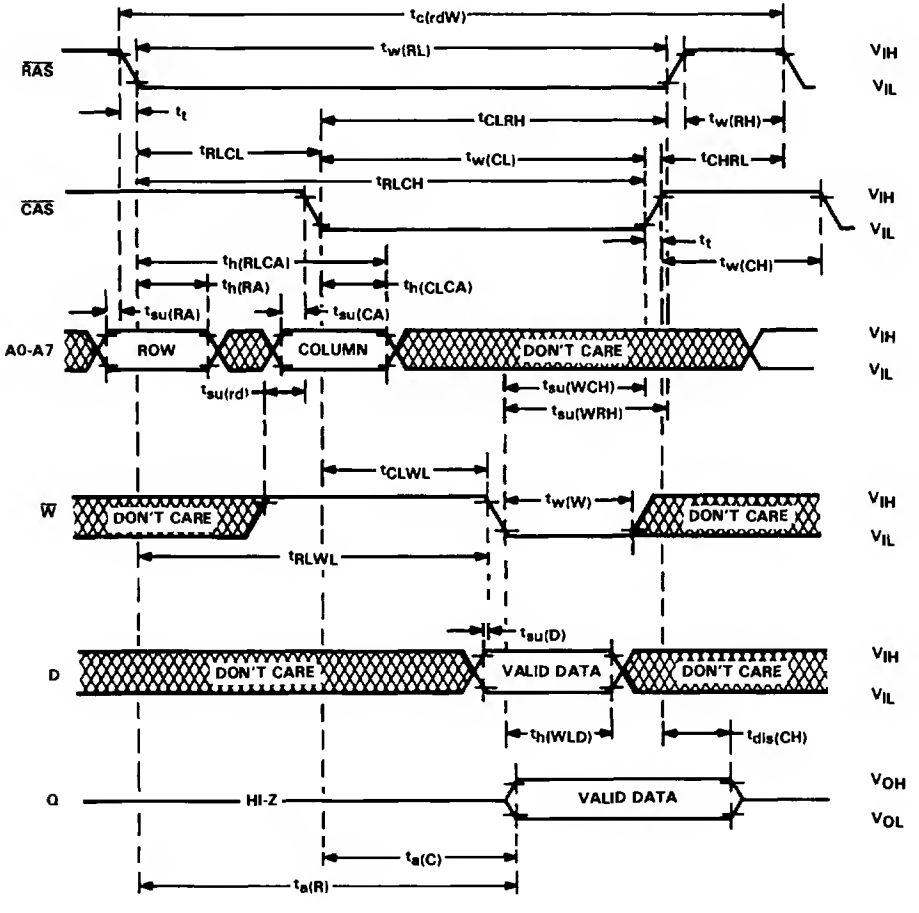


write cycle timing

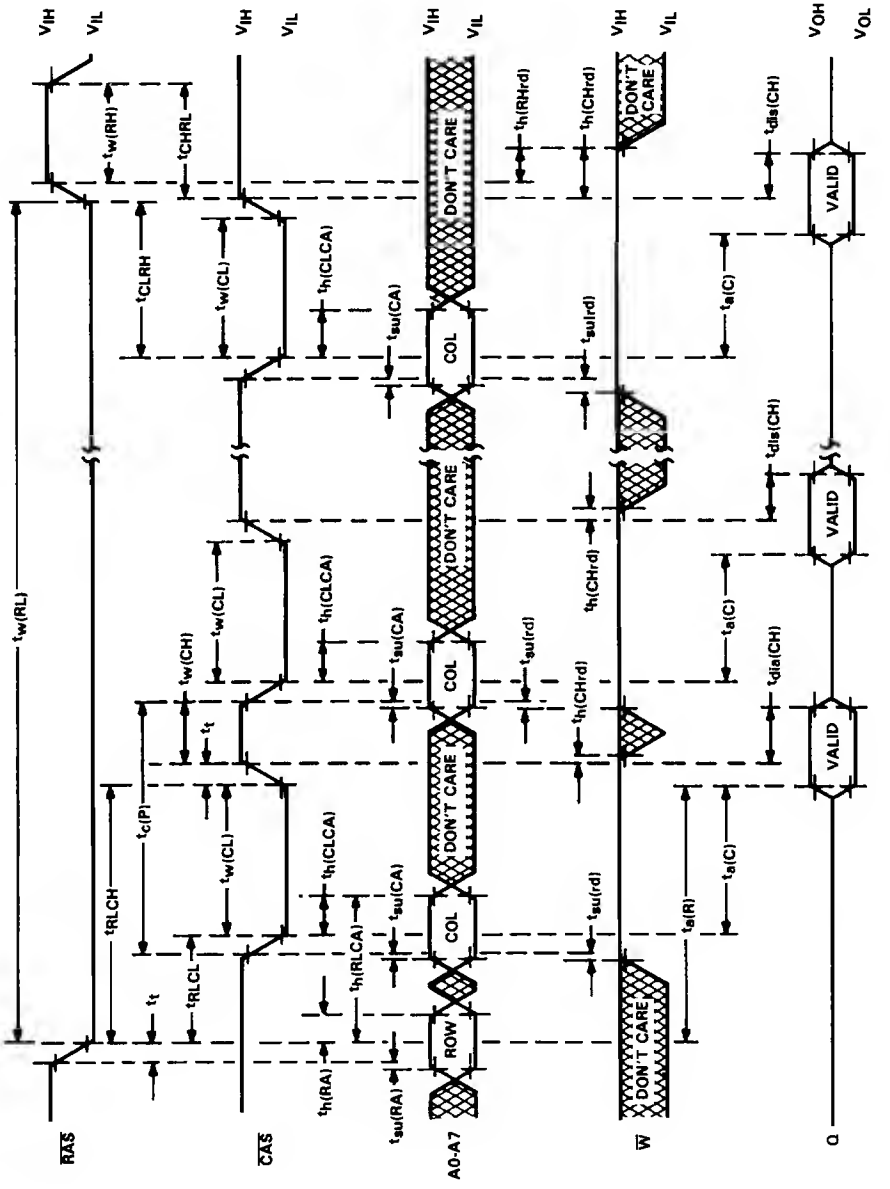


† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-modify-write cycle timing

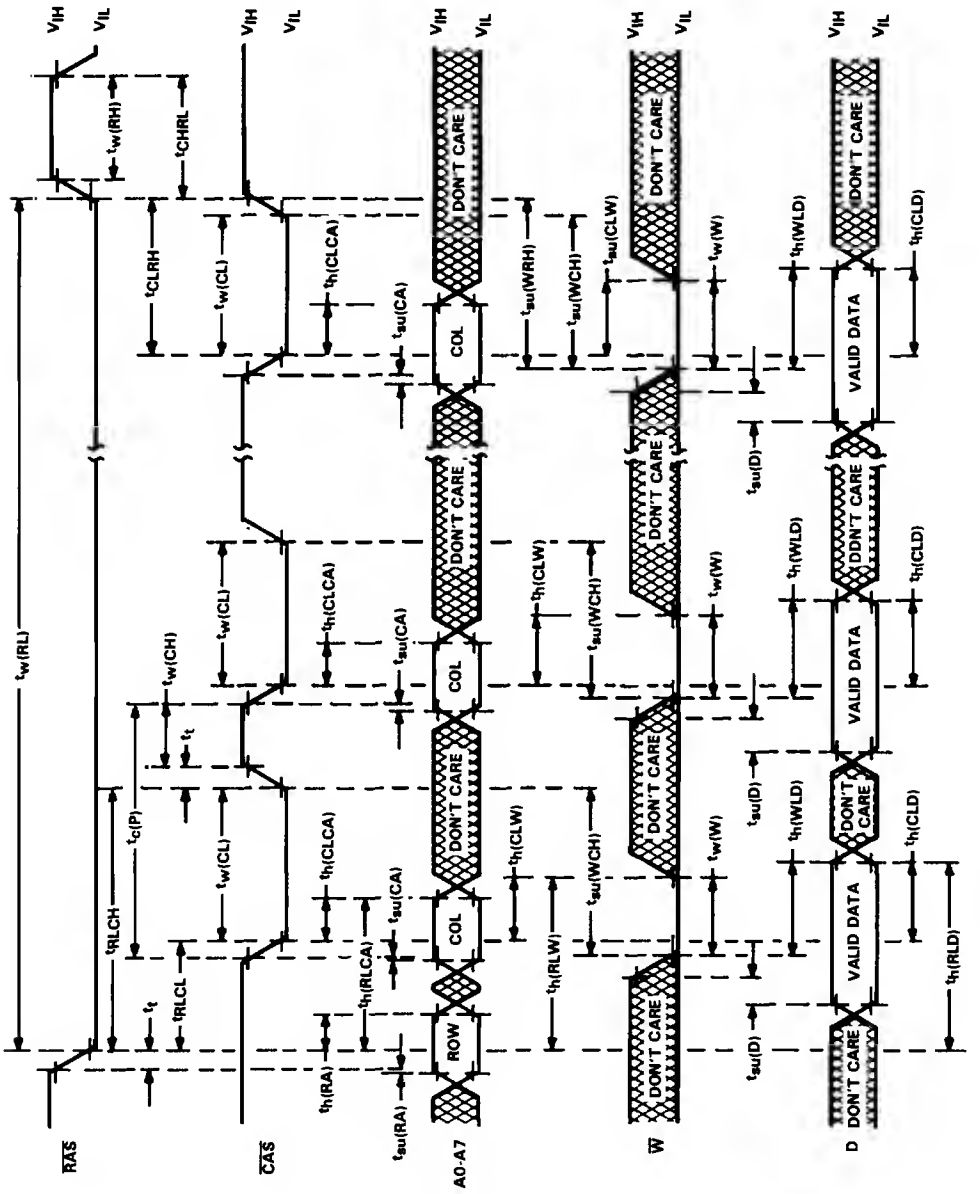


page-mode read cycle timing



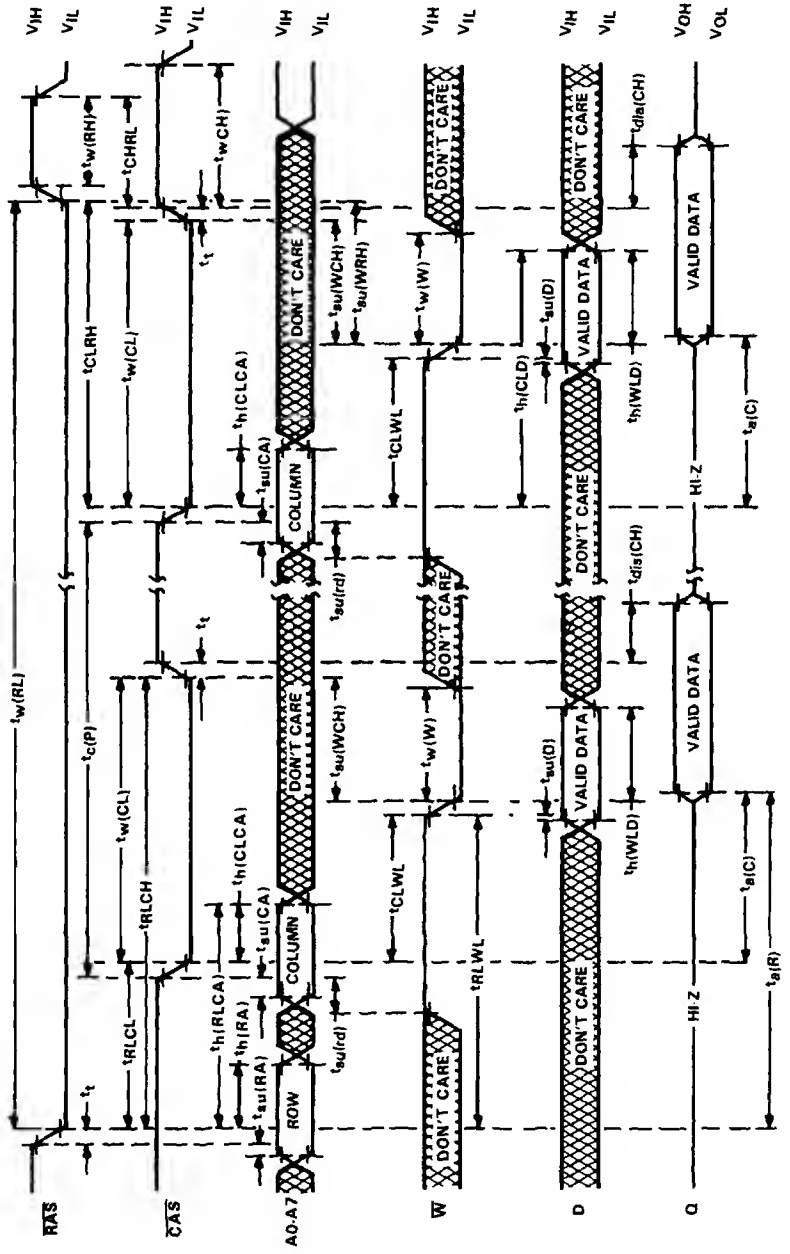
NOTE 2: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



NOTE 3: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing



NOTE 4: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

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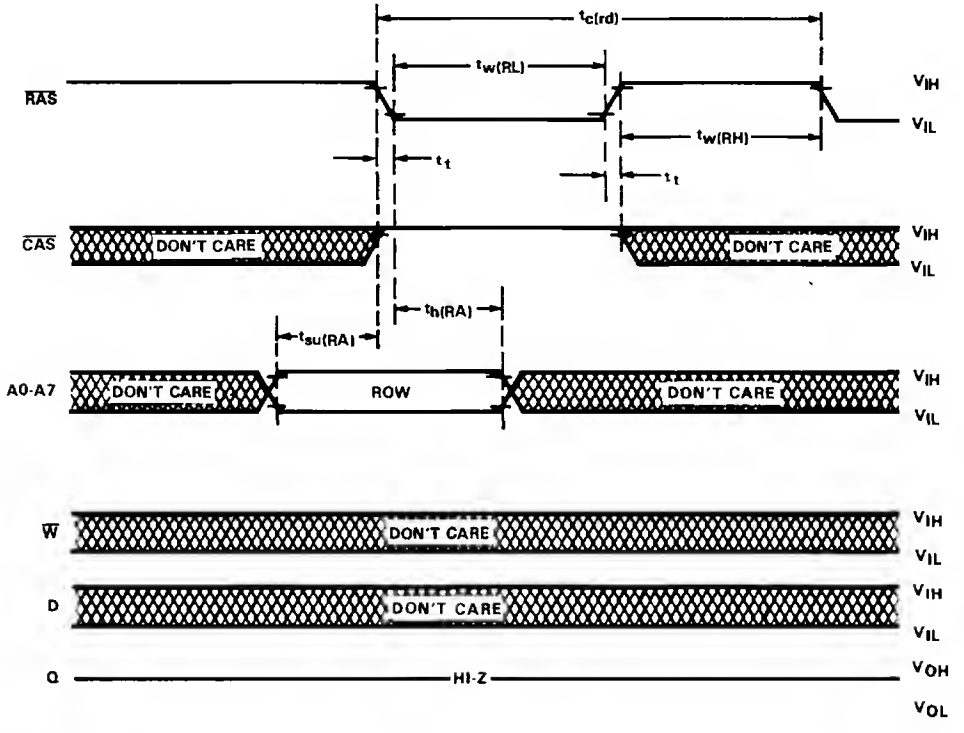
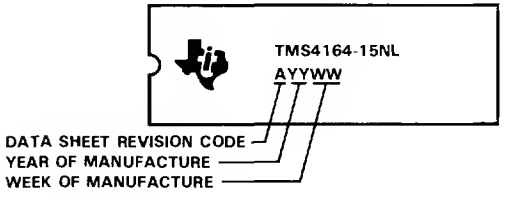
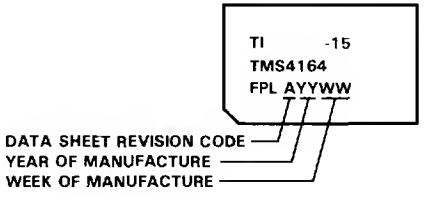
$\overline{\text{RAS}}$-only refresh timing



device symbolization

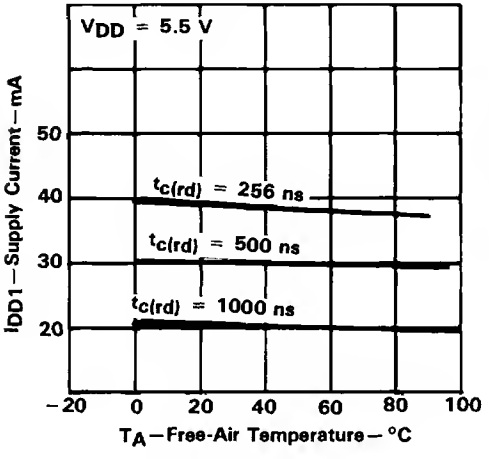
This data sheet is applicable to all TI TMS4164 Dynamic RAMs with the code "A" to the left of the date code as shown below:



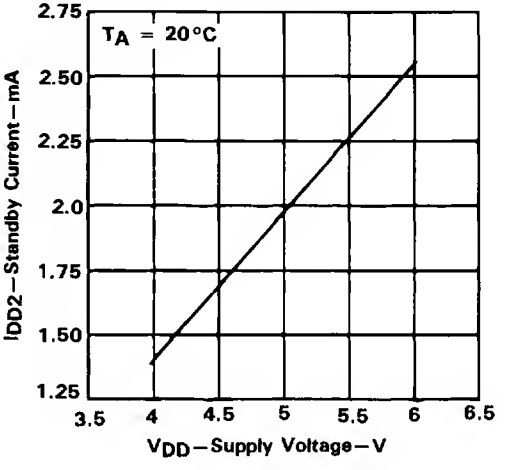


TYPICAL CHARACTERISTICS

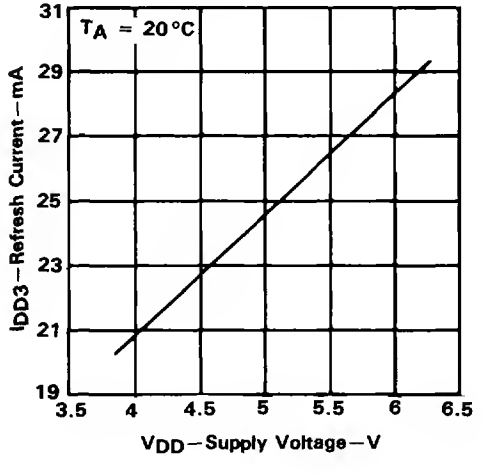
TYPICAL SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



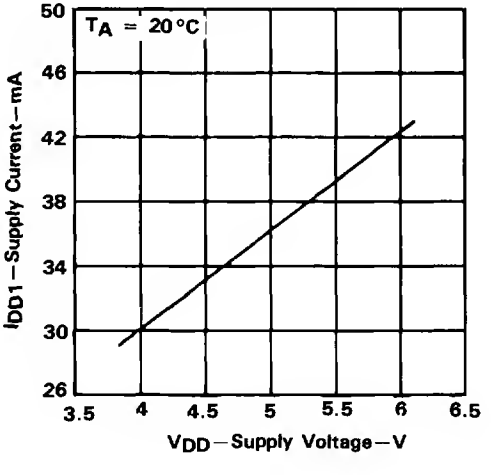
TYPICAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE



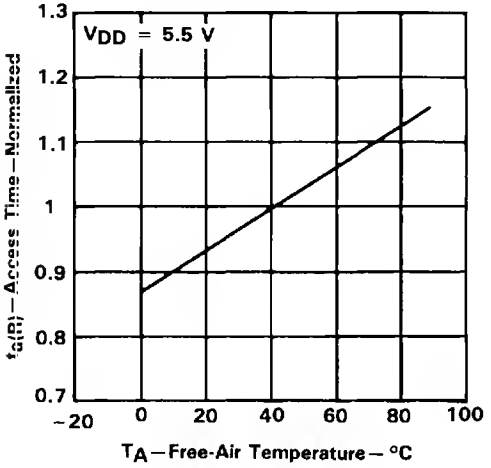
TYPICAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE



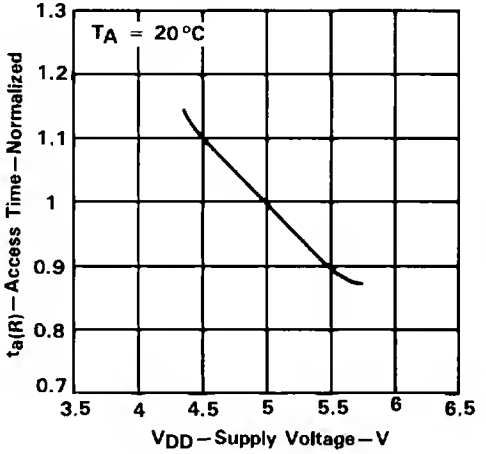
TYPICAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE



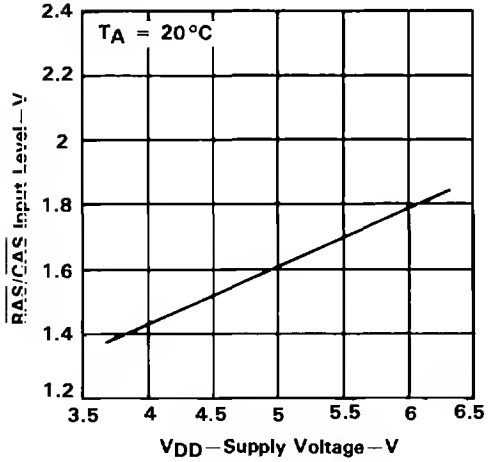
ACCESS TIME
vs
FREE-AIR TEMPERATURE



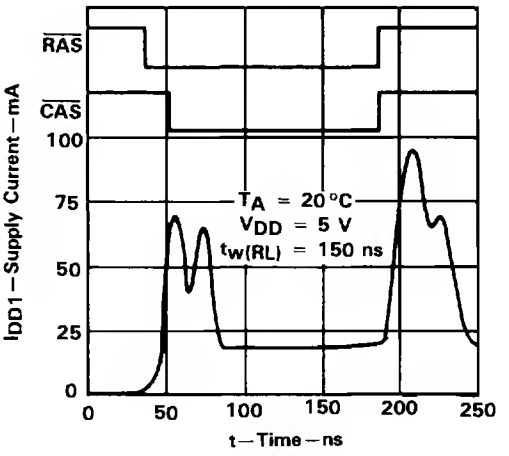
ACCESS TIME
vs
SUPPLY VOLTAGE



$\overline{RAS}/\overline{CAS}$ INPUT LEVEL
vs
SUPPLY VOLTAGE



AVERAGE CURRENT
DURING AN OPERATING CYCLE



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Dynamic RAMs